

Substitute for form 1449A&B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Complete if Known		
			<i>Application Number / Confirmation Number</i>		
			10/783,589 /1594		
			<i>Filing Date</i>		
			02/20/2004		
			<i>First Named Inventor</i>		
		Kevin T. Look			
<i>Art Unit</i>		2800			
<i>Examiner Name</i>		Unknown			
Sheet	1	of	4	<i>Attorney Docket Number</i>	X-1462-2P US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ¹ (if known)			
		US-2003/0030326	02/13/2003	Shenai et al.	
		US-2003/0218478	11/27/2003	Sani et al.	
		US-2005/0091547	04/28/2005	Hanrieder et al.	
		US-2005/0201174	09/15/2005	Klein	
		US-2006/0053246	03/09/2006	Lee, Schweiray Joseph	
		US-2006/0069651	03/30/2006	Chung et al.	
		US-2006/0202713	09/14/2006	Sergey Shumarayev, San	
		US-2007/0001720	01/04/2007	Li et al.	
		US-5,362,989	11/08/1994	Hennedy	
		US-5,519,663	05/21/1996	Harper et al.	
		US-5,583,457	12/10/1996	Horiguchi	
		US-5,615,162	03/25/1997	Houston	
		US-5,682,107	10-28-1997	Tavana et al.	
		US-5,682,107	10/28/1997	Tavana	
		US-5,801,548	09/01/1998	Lee et al.	
		US-5,811,962	09/22/1998	Ceccherelli	
		US-5,832,286	11/03/1998	Yoshida	
		US-5,914,873	06/22/1999	Blish	
		US-5,946,257	08/31/1999	Keeth	
		US-5,958,026	09/28/1999	Goetting et al.	
		US-6,148,390	11/14/2000	MacArthur	
		US-6,160,418	12/12/2000	Burnham, James L.	
		US-6,169,419	01/02/2001	De et al.	
		US-6,208,171	03/27/2001	Kumagai et al.	
		US-6,384,626	05/07/2002	Tsai et al.	
		US-6,466,049	10-15-2002	Diba et al.	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449A&B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Complete if Known		
			<i>Application Number / Confirmation Number</i>		
			10/783,589 /1594		
			<i>Filing Date</i>		
			02/20/2004		
			<i>First Named Inventor</i>		
		Kevin T. Look			
<i>Art Unit</i>		2800			
<i>Examiner Name</i>		Unknown			
<i>Sheet</i>	2	<i>of</i>	4	<i>Attorney Docket Number</i>	X-1462-2P US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ⁽¹⁾⁽²⁾⁽³⁾			
		US-6,489,804	12/03/2002	Burr, James B.	
		US-6,583,645	06/24/2003	Bennett et al.	
		US-6,631,502	10/07/2003	Buffet et al.	
		US-6,710,621	03/23/2004	Farnworth	
		US-6,711,719	03/23/2004	Cohn et al.	
		US-6,747,478	06/08/2004	Madurawe, Raminda U.	
		US-6,839,888	01/04/2005	Gupta, Vidyabhusan	
		US-6,885,563	04/26/2005	Panella	
		US-6,920,627	07/19/2005	Blodget et al.	
		US-6,936,917	08/30/2005	Lopata et al.	
		US-6,950,998	09/27/2005	Tuan, Tim	
		US-6,960,934	11/01/2005	New, Bernard J.	
		US-6,981,160	12/27/2005	Thaker et al.	
		US-7,003,620	02/21/2006	Avraham et al.	
		US-7,078,932	07/18/2006	Swami	
		US-7,080,341	07/18/2006	Eisenstadt et al.	
		US-7,098,689	08/29/2006	Tuan et al.	
		US-7,109,748	09/19/2006	Liu et al.	
		US-7,112,997	09/26/2006	Liang et al.	
		US-7,135,886	11/14/2006	Schlacter	
		US-7,170,315	01/30/2007	Bakker et al.	
		US-7,313,708	12/25/2007	Oshins	
		US-7,345,944	03/18/2008	Jenkins	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449A&B/PTO			Complete if Known		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)			<i>Application Number / Confirmation Number</i>		
			10/783,589 /1594		
			<i>Filing Date</i>		
			02/20/2004		
			<i>First Named Inventor</i>		
			Kevin T. Look		
			<i>Art Unit</i>		
			2800		
			<i>Examiner Name</i>		
			Unknown		
<i>Sheet</i>	3	<i>of</i>	4	<i>Attorney Docket Number</i>	
				X-1462-2P US	

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume/issue number(s), publisher, city and/or country where published.	T ²	
		ALLEN/HOLBERG, Chapter 10: "Bandgap Voltage Reference"; April 12, 2000; downloaded on January 3, 2006 from www.ece.utexas.edu/~holberg/lecture_notes/bandgap.pdf; pp. 1-5.		
		INTEL CORPORATION, "Intel PXA27x Processor Family Power Requirements", Application Note, 2004, pages 1-36, available from Intel Corporation (Santa Clara) Corporate Office, 2200 Mission College Blvd., Santa Clara, California 95052-8119.		
		Microchip Technology Inc.; "Micropower Voltage Supervisors"; MCP102/103/121/131; Copyright 2005; downloaded on January 3, 2006 from www1.microchip.com/downloads/en/DeviceDoc/21906b.pdf; pp. 1-28		
		NOWKA, KEVIN J., A32-bit PowerPC System-on-a-Chip With Support For Dynamic Voltage Scaling and Dynamic Frequency Scaling", November 2002, pp. 1441-1447, Vol. 37, No. 11, IEEE Journal of Solid-State Circuits, Available from IEEE; 3 Park Avenue, 17th Floor, New York, NY 10016-5997.		
		Texas Instruments - Datasheet BQ4011 (32x8 nonvolatile SRAM) 05/99 Pgs 1-15.		
		Texas Instruments (BenchMARq) - Datasheet BQ4011 (32x8 nonvolatile SRAM) 08/93 Pgs 1-11.		
		XILINX, INC., "Spartan-3L Low Power FPGA Family", Preliminary Product Specification, DS313, September 15, 2005, v1.1, pages 1-10, available from Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124-3L		
		XILINX, INC., "Virtex-II Pro Platform FPGA Handbook"; published October 14, 2002; available from Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124; pp. 19-71.		
		11/502,939 filed 08/11/06, TUAN, TIM, et al., entitled "Disabled Unused/Inactive Resources in Programmable Logic Devices for Static Power Reduction", Xilinx, Inc., San Jose, CA 95124		
		11/326,542 filed 01/04/06, JACOBSON, NEIL G. et al., entitled "Method and Mechanism for Controlling Power Consumption of an Integrated Circuit", Xilinx, Inc., San Jose, CA		

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449A&B/PTO			Complete if Known		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)			<i>Application Number / Confirmation Number</i>		
			10/783,589 /1594		
			<i>Filing Date</i>		
			02/20/2004		
			<i>First Named Inventor</i>		
			Kevin T. Look		
			<i>Art Unit</i>		
			2800		
			<i>Examiner Name</i>		
			Unknown		
Sheet	4	of	4	<i>Attorney Docket Number</i>	
			X-1462-2P US		

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume/issue number(s), publisher, city and/or country where published.	T ²	
		11/325,888 filed 01/04/06, TUAN, TIM, entitled "Programmable Low Power Modes For Embedded Memory Blocks", Xilinx Inc., San Jose, CA		
		11/268,265 filed 11/04/05, RAHMAN, ARIFUR, et al. entitled "Implementation of Low Power Standby Modes For Integrated Circuits", Xilinx, Inc., San Jose, CA		
		10/971,934 filed 10/22/04, JENKINS, JESSE H. IV, entitled "Low Power Zones For Programmable Logic Devices", Xilinx, Inc., San Jose, CA 95124		
		10/783,216 filed 02/20/2004, TUAN, TIM et al., entitled "Tuning Programmable Logic Devices for Low-Power Design Implementation", Xilinx, Inc., San Jose, CA 95124		

Examiner Signature		Date Considered	
-----------------------	--	--------------------	--

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.